Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

ANP044B BY ANDREAS NADLER

1. INTRODUCTION

The technical literature, including, for example, our “Trilogy of Magnetics” and the IC data sheets, provides hardware developers with all manner of useful tips regarding the design of switching controllers. From the selection of the appropriate power inductor, input/output capacitors, MOSFETs, and Schottky diodes, application examples ranging all the way to a specimen PCB layout are presented that demonstrate how an EMC-compliant design can be realized.

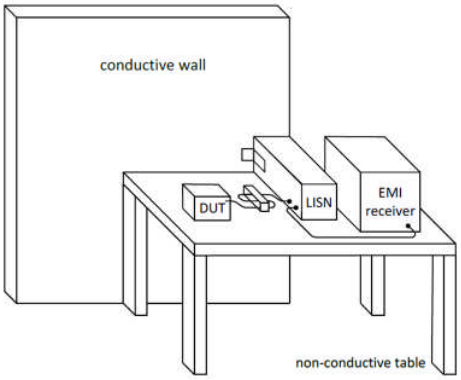


Figure 1: Test set-up for interfering voltage

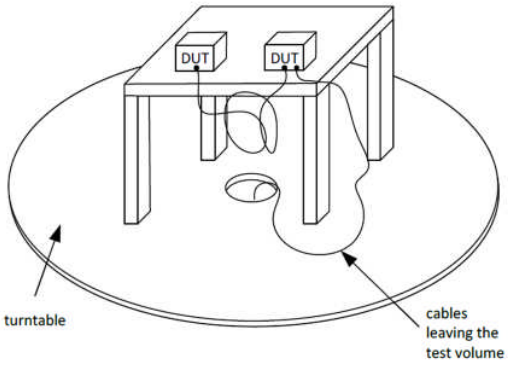


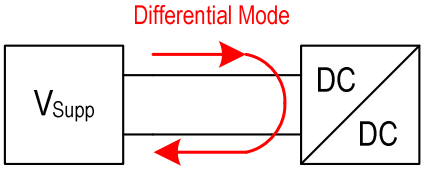
Figure 2: Test set-up for interference-field strength with turntable

These literature, however, describes hardly any comparative EMC measurements that prove the efficiency of the measures taken. Virtually every state-of-the-art PCB contains one or several DC/DC converters in one form or another. This is why before/after comparative EMC measurements of discretely integrated DC/DC converters give almost all hardware developers an interesting opportunity to deepen his/her knowledge in this area. Since we at Würth Elektronik eiSos are right at home in the EMC area, equipped with the suitable measurement instruments, and are more than glad to assist electronics developers, we have written this Application Note to describe these comparisons in detail.

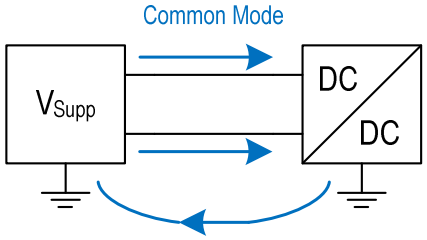
2. PRINCIPLES

2.1. TYPES OF INTERFERENCE

To understand the way in which radiated and conducted interferences can occur, a distinction must be drawn between the type of interference signal involved (common mode or differential mode) and to properly identify the feedback paths.



- Differential-mode current is phase-shifted by 180°
- Interference current loop closes via outward and return conductor
- Suppression with LC, T, Π filter



- Common-mode current is in phase
- Interference current loop closes via the ground wire
- Suppression with current-compensated choke

Figure 3: Difference between common-mode and differential-mode signal

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When it comes to designing an EMC-compliant layout, it is necessary to know just why and where the corresponding EMC interferences can arise. In the case of switching controllers, measurements in the EMC chamber (interference-field strength acc. to e.g. EN 61000-4-3) frequently show a broad-band interference spectrum ranging between 30 MHz and 400 MHz. One of the causes for this is the steep MOSFET switching edge (depending on the rise time, with a frequency spectrum of up to several hundred MHz), which for instance with the MOSFET output capacitance C_{DS}, the junction capacitance, and the reverse recovery capacitance of the Schottky diode and the parasitic conductor-track inductances cause high-frequency LC circuits. When a single ground conductor track is not kept to a low impedance, or when single conductor-track wire conduct two currents and cause feedback in the common impedance, common-mode interferences can potentially be expected in the design. These interferences will then decouple capacitively in the direction of the interference source to form a high-frequency closure of the interference current.

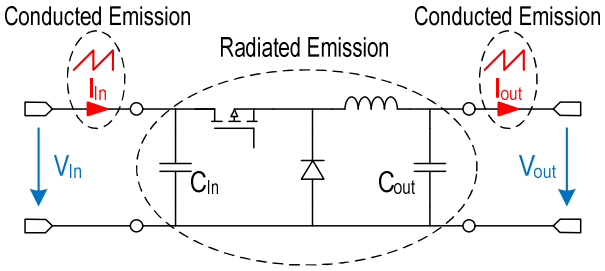


Figure 4: Potential sources for conducted and radiated emission

The measurement of the interference voltage (acc. to. e.g. CISPR 16-2-1) reveals the switching frequency of the controller and its harmonic waves up to a level of 10 MHz. Depending on the shielding and the length of the wire, these occur as a mixture of common-mode and differential-mode interference signals. The cause of the differential-mode interference signals lies in the discontinuous current consumption of the MOSFET, which then causes a drop in voltage at the ESR of the input and output capacitors.

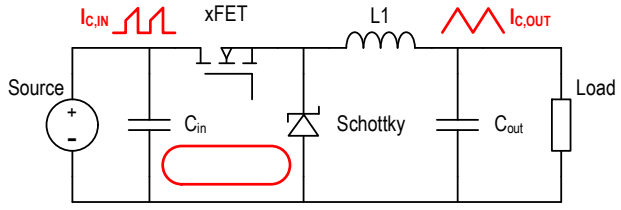


Figure 5: critical current loop buck converter

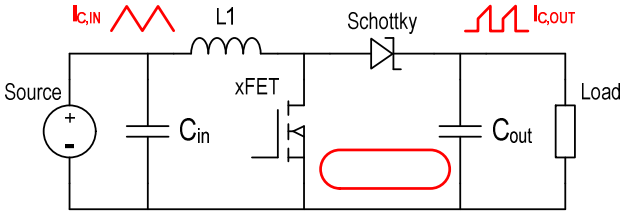


Figure 6: critical current loop boost converter

Beyond considering the impact of components and layout regarding the interference voltage, it is also necessary to bear in mind that the topologies of the switching controllers differ in terms of their potential to cause interferences more at the input or the output. As shown in Figures 5 and 6, in the boost converter it is the output that is the more critical aspect, since here the power inductor acts as a "current brake" (di/dt) between the MOSFET and the input. The buck converter, on the other hand, plays a more critical role at the input, since in this topology the power inductor is situated between the MOSFET and the output. This clearly demonstrates that a buck converter requires an input filter and a boost converter an output filter to suppress the discontinuous current curve. This does not mean, however, that the other, less critical loop should be neglected.

2.2. INPUT FILTERS, INTERFERENCE VOLTAGE

Modern converters generally feature switching frequencies from 250 kHz up to 4 MHz. LC filters are particularly suited to bring the fundamental wave and its harmonics in the spectrum under control. These filters are capable of achieving a suppression of up to 40 dB per decade, and also enable filter cut-off frequencies down to the low kHz range to be realized.

Filter resonance frequency:

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{filter} \cdot C_{filter}}}$$

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An appropriate rule of thumb for practical applications is to set the cut-off frequency of the filter to approx. one tenth of the frequency of the switching controller, thus achieving a suppression of the spectral amplitude by approx. 40 dB at the switching frequency (fundamental). In the case that the EMC levels are still too high, the cut-off frequency should also be set even lower, a measure that, however, entails larger components or a poorer R_{DC} in the filter inductance.

Filter inductance at the specified filter capacity:

$$L_{filter} = \frac{1}{(2 \cdot \pi \cdot 0{,}1 \cdot f_{sw})^2 \cdot C_{filter}}$$

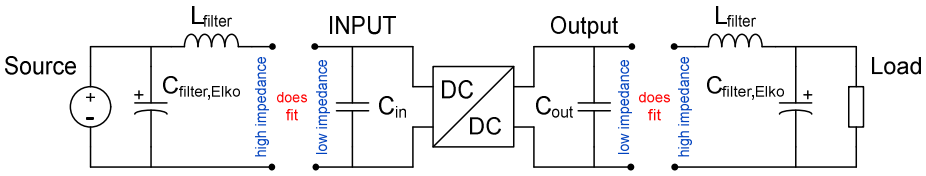


Abbildung 7: Darstellung der Ein-& Ausgangs Beschaltung für die Filterung von Gegentaktstörern

Suitable filter inductances in this regard are e.g. ones from the WE-LQS, WE-LHMI or WE-MAPI series. The criteria for selection include the maximum current-carrying capacity (ampacity) and the self-resonant frequency (SRF), which should be higher than the spectrum to be filtered. Care should be taken not to exceed the frequency spectrum with the inductively determined coil impedance, with a sufficient interval to the SRF, since this may be subject to fluctuations for production-related causes. In the practical area, generally inductance values ranging from 1 µH to 22 µH are applied, since these components already exhibit a sufficiently high impedance in the frequency range of relevance regarding differential-mode interference signals. In this inductance range, it is also possible to select components that in many cases offer a well-balanced compromise between size, ampacity, and costs.

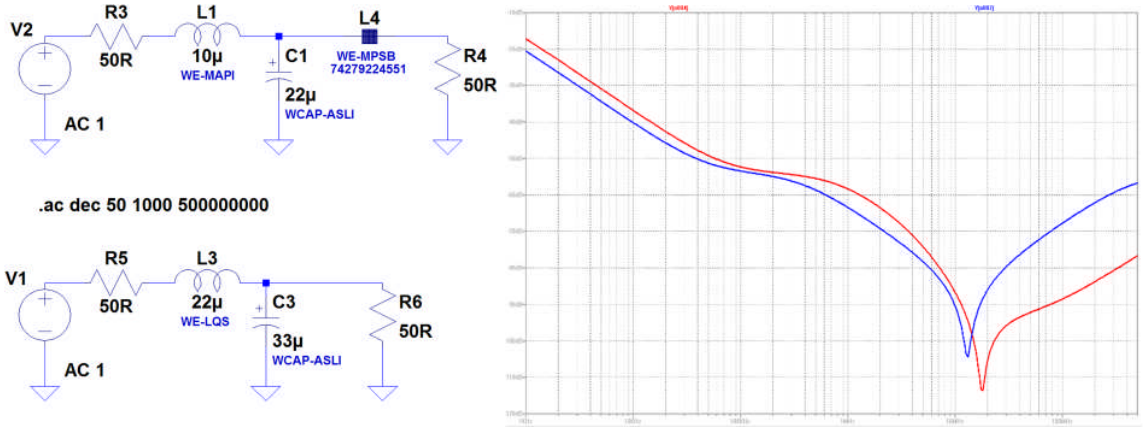


Figure 8: Simulated (LT Spice) suppression of a pure LC filter (22µH + 33µF blue) and a T filter (10µH + 22µF + MPSB 74279224551 red

An appropriate measure for increasing the impedance of the input filter in particular in the frequency range over 10 MHz (Figure 8) is to complement the LC filter by a WE-MPSB ferrite. This ferrite is substantially superior to conventional ferrites in terms of maximum pulse current (see ANP028 for details) and thus constitutes an excellent choice when it comes to the suppression of high-frequency DC power-supply systems. What's more, the inductor and the capacitor can also be dimensioned slightly smaller. As is the case for all SMD ferrites, when choosing the WE-MPSB the dependence of the impedance on DC current must also be taken into consideration.

The higher the switching frequency of the converter, the smaller not only the power choke and input/output capacitors can be made, but also the LC filters, since this enables the selection of a higher cut-off-frequency. In addition, smaller passive components also make it easier to design a more compact CB layout, which in turn promises potentially better EMC characteristics.

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Suitable filter capacitors in this regard are small SMD electrolytic capacitors, e.g. from the WCAP-ASLI series. Values of 10 µF to 100 µF are standard. The objective in the design procedure should be to keep the filter inductance as small as possible while at the same time enlarging the filter capacity. This measure has a positive impact on the efficiency, and also reduces the risk of instability due to the negative input impedance.

When MLCCs (e.g. WCAP-CSGP) with class 2 ceramics (e.g. X5R/X7R) are used as the filter capacitors, the calculated filter cut-off frequency will deviate to a substantially greater degree in operation, or the residual voltage ripple will increase to a greater degree than the pure tolerance specification would suggest.

Class 2 ceramics exhibit a strong dependency on the capacity, subject to the following factors of influence:

- Voltage (DC Bias Derating)
- Ageing
- Frequency
- Temperature

This is why it is preferable to use aluminium-electrolyte capacitors when designing filters for switching controllers. In addition, their relatively high ESR has a positive effect, since this factor has a better dampingeffect on the quality of the LC circuit than that produced by a low ESR type.

In modern switching controllers, class 2 MLCCs are generally used as input and output capacitors for the following reasons:

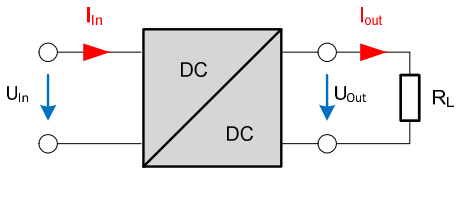
- Low ESL (current can be transported swiftly)
- Low ESR (high RMS ampacity and low residual voltage ripple)
- Space-saving effect thanks to high volume capacity of class 2 ceramics

However, when MLCCs are used as input capacitors in combination with a filter inductance or a parasitic lead inductance, in the event of voltage transients (e.g. a drop in the input voltage), oscillations may occur at the switching controller input. Such oscillations are caused by the so-called negative input resistance in combination with the LC circuit that is produced. Here the filter inductance and the MLCC input capacitor combine to produce an oscillating circuit with a magnified resonance peak. Since a negative impedance by nature does not absorb energy, but rather is capable of supplying energy, together with the parasitic and intentionally used inductances this results in the formation of an undesirable oscillating circuit. Here the LC circuit is fed by a residual energy that the converter does not absorb during the transient. Due to the switch at the input, the “C” is an absolute necessity. The “L”, however, can be due not only to a filter inductance, but also to the lead / layout / ESL. This means that undesirable oscillations can occur even in cases in which filters are not involved.

$$P_{in} \sim P_{out}$$

$$U_{in} \cdot I_{in} = U_{out} \cdot I_{out}$$

$$R_{in} = \frac{\Delta U}{\Delta I} = \frac{-U_{in}^2}{P_{out}}$$



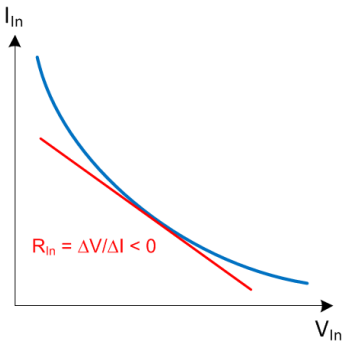


Fig. 9: Since the output remains constant even in the case of a drop in the input voltage, it is logical that the input current must rise. This results in a brief negative input resistance during this voltage transient.

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This negative input impedance can result in a series of problems:

- Destabilization of the output regulation loop when the frequency spectrum of the negative impedance at the input overlaps the bandwidth of the control loop.
- Voltage overshoots in the event of resonance, capable of causing damage to active and passive components.
- Cause of other EMC interference signals

The risks posed by a negative impedance are greatest when the input voltage is lowest and thus the input current is largest.

The best method currently available to avoid these undesirable effects is to actively suppress the LC circuit. This can be achieved by using an SMD resistor (this resistor has a low self-inductance) in series with a capacitor that blocks the DC voltage (cf. Fig. 10). The aim of this approach should be to achieve a resonant circuit factor of Q=1 or a damping factor ζ (zeta) of 0.707. In many cases, an electrolytic capacitor with a correspondingly high ESR is used instead. This is frequently, however, a “shot in the dark“, since the ESR is a value that is strongly dependent on frequency and temperature, and the developer often does not yet know in which frequency spectrum the undesirable oscillations will occur. Notwithstanding this, an electrolytic capacitor can be used as a “filter capacitor” in the manner shown in Fig. 9.

The following general statement applies: the lower the “L” and the higher the “C”, the lower the hazards of the negative input impedance, since their contribution $|Z_{in}|$ drops accordingly.

Stability criteria:

$$\frac{L_{filter}}{C_{input} \cdot R_{damp}} \ll R_{in} \qquad |Z_{out,filter}| \ll |Z_{in,smps}|$$

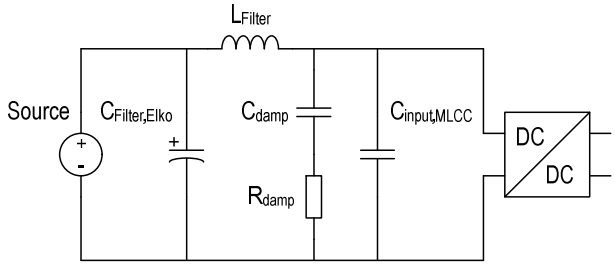


Figure 10: Measures for filter suppression: SMD resistor in series with a capacitor

The damping capacitor should be approx. four times larger than the input capacitor to avoid any conflict with the input impedance. The damping capacitor must exhibit a lower impedance than the damping resistor at the resonance frequency to ensure that the damping resistor is capable of effectively attenuating the resonance peak of the filter.

$$n = \frac{C_{damp}}{C_{input}} \qquad \zeta = \frac{n+1}{n} \cdot \frac{L_{filter}}{2 \cdot R_{damp} \cdot \sqrt{L_{filter} \cdot C_{input}}}$$

R_{damp}. The degree to which a stable design has been achieved can be simply measured using a current clamp, closely monitoring the amplitude of the current in the input capacitor over the entire dynamic range of the converter. When this current curve corresponds to the anticipated transients through the input capacitor, the converter is stable. In the event, however, that a too high amplitude occurs that does not correspond to the expected area of operation, the corresponding damping measures must be taken. In the following switching examples, such a damping resistor has not been used.

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2.3. OUTPUT FILTERS

Output filters are frequently used to reduce the residual ripple of the output voltage further still. In the case that the drop in voltage over the filter inductance cannot be ignored, the output voltage must be captured downline from this filter and not, as is usually the case, at the output capacitor itself.

When a design makes use of an output filter that lies within the voltage feedback, the relevant frequency points should be considered. In this case, the output filter must be damped in all events so as not to endanger the stability of the control loop. In addition, the compensating circuit of the controller must also be recalculated, since the filter constitutes an additional pole.

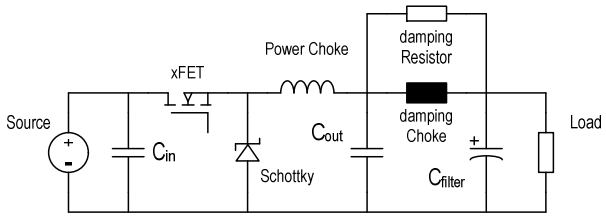


Figure 11: Damping of the output filter with a parallel resistor to the filter inductance

Damping resistance output filter: $R_{damp} = \sqrt{\frac{L_{filter}}{C_{filter}}}$

Typical values for a filter inductance at the output are 0.47 µH to 2.2 µH. In addition, the R_{DC} should be small and the self-resonance frequency as high as possible. The WE-PMCI, WE-MAPI, WE-HCI or WE-LHMI series are excellently suited for this task. An important aspect in the selection of the R_{damp} in this case is that this must be considerably larger than the R_{DC} of the filter inductance so as not to reduce the damping of the filter.

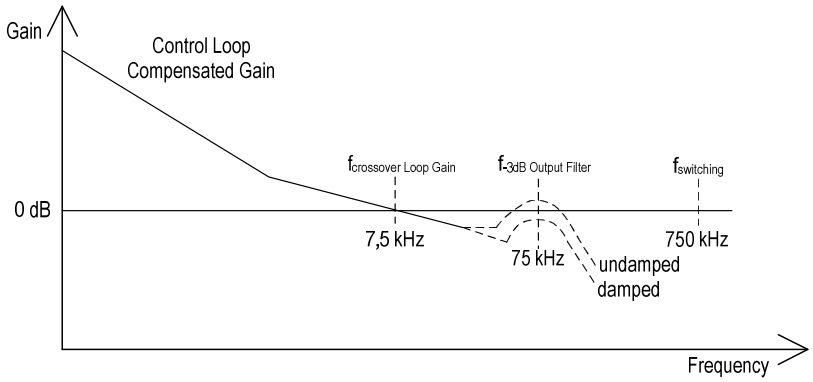


Figure. 12: Setting of the various frequencies as a factor of the circuitry and switching frequency

Instead of a classic inductance, here it is also possible to use a WE-MPSB ferrite. Suitable for use as filter capacitors here are compact SMD electrolytic capacitors of the WCAP-ASLL and WCAP-ASLI series in the capacity spectrum from 10 µF to 100 µF.

Here, too, ceramic capacitors using class 2 ceramics should also not be used in the design of the output filter, for the reasons already given above.

Figure 12 presents an example of how the frequencies can be set in a switching controller with an operating frequency of 750 kHz for:

- LC output filters -3 dB cut-off frequency (damped)
- 0 dB gain crossover frequency of the compensated control loop

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Since the output filter in most cases is set at one tenth of the switching frequency, the 0dB crossover frequency of the control-loop compensated gain must be set at least one decade below this figure, since the phase already begins to rotate at this point in time, thus reducing the phase reserve in the system.

In all boost converters that work in continuous mode (voltage mode and CCM), the right half plane zero (RHPZ) factor must also be considered. This constitutes a further limiting factor for the maximum control-loop bandwidth. Its distance from the converter pole in the frequency spectrum must also be at least one decade on account of the phase rotation.

$$\text{Right Half Plane Zero:} \quad f_{RHPZ} = \frac{R_{load}}{2\pi \cdot L}\left(\frac{U_{in}}{U_{out}}\right)^2$$

$$\text{Converter pole:} \quad f_0 = \frac{1}{2\pi\sqrt{L_{power} \cdot C_{out}}} \cdot \frac{V_{in}}{V_{out}}$$

Distance in the frequency spectrum for a stable control loop:

$$\frac{f_{RHPZ}}{f_0} > 10 \ (\triangleq \text{one decade})$$

EMC measurements of various designs

The following section describes two designs using the same boost converter. Design (1) here is representative of a “critical” design, while Design (2) stands for a “good” design. The circuit diagram and the choice of components used in Design (1) were drawn up on the basis of a specimen application taken from the data sheet of the IC supplier.

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2.4. CIRCUIT DIAGRAM CRITICAL DESIGN (1)

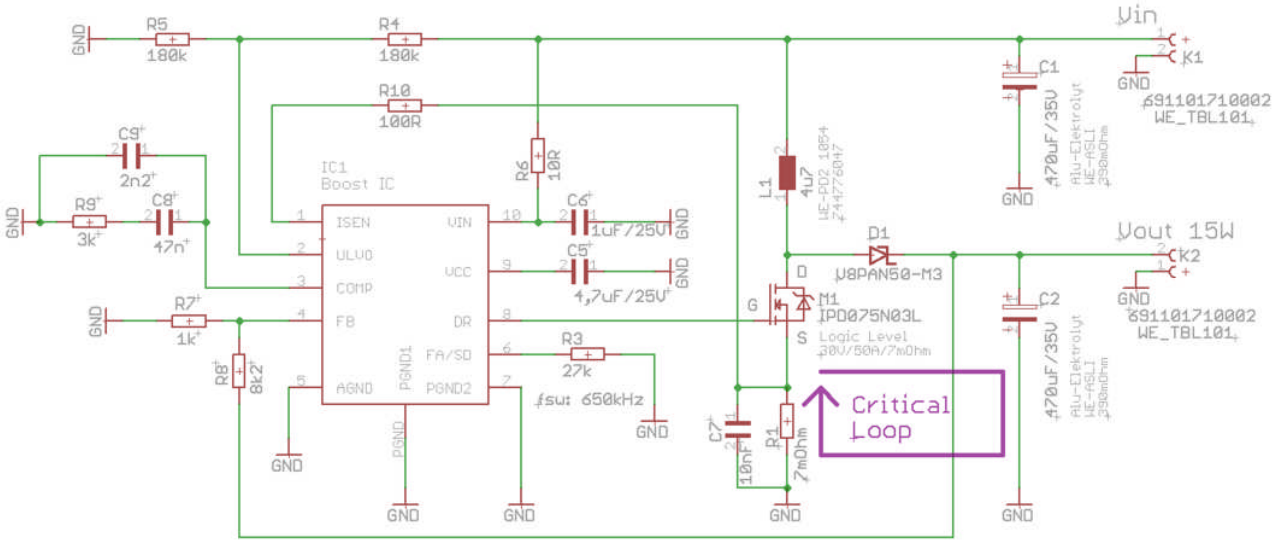


Figure 13: Circuit diagram of a critcal design (Design 1) with U_{in} = 9 V, U_{out} = 12 V, I_{out} = 1.25 A, f_{sw} = 650 kHz

Initial analysis of the circuit diagram for Design (1):

-
- No additional filters at the input and output of the boost converter.
- No series gate resistor at the external MOSFET.
- Unshielded power choke.
- No separation between AGND and PGND

Initial analysis of the circuit-board layout of Design (1):

- The PGND PTOs of the input and output capacitors (C1 & C2), IC, and shunt R1 are too distant from each other, meaning that there is a very large and critical current loop.
- The C5 and C6 blocking capacitors are too far from the IC.
- All power connections are routed with connector tracks that are too thin and too long.
- Connection (exception: C_{OUT} = C2) and routing of the feedback connector track highly unfavourable.
- No separation between AGND and PGND.
- Too few Vias are placed, especially regarding the PGND connections.
- Stub cable from C1 to the input wire.

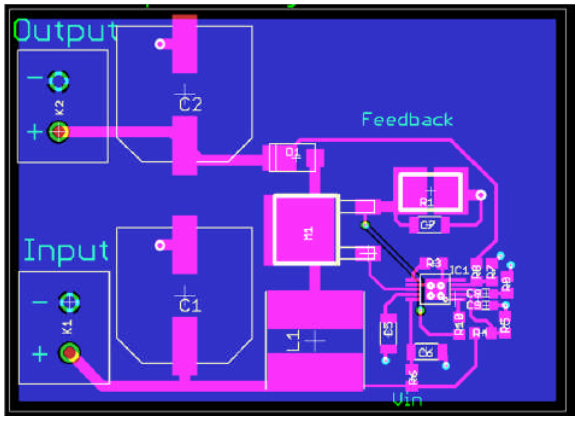


Figure 14: Circuit-board layout of the critical design (Design 1)

In the light of the obvious deficiencies, a second design (Design 2) was developed to test its efficiency in terms of the EMC.

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2.5. CIRCUIT DIAGRAM „BETTER“ DESIGN (DESIGN 2)

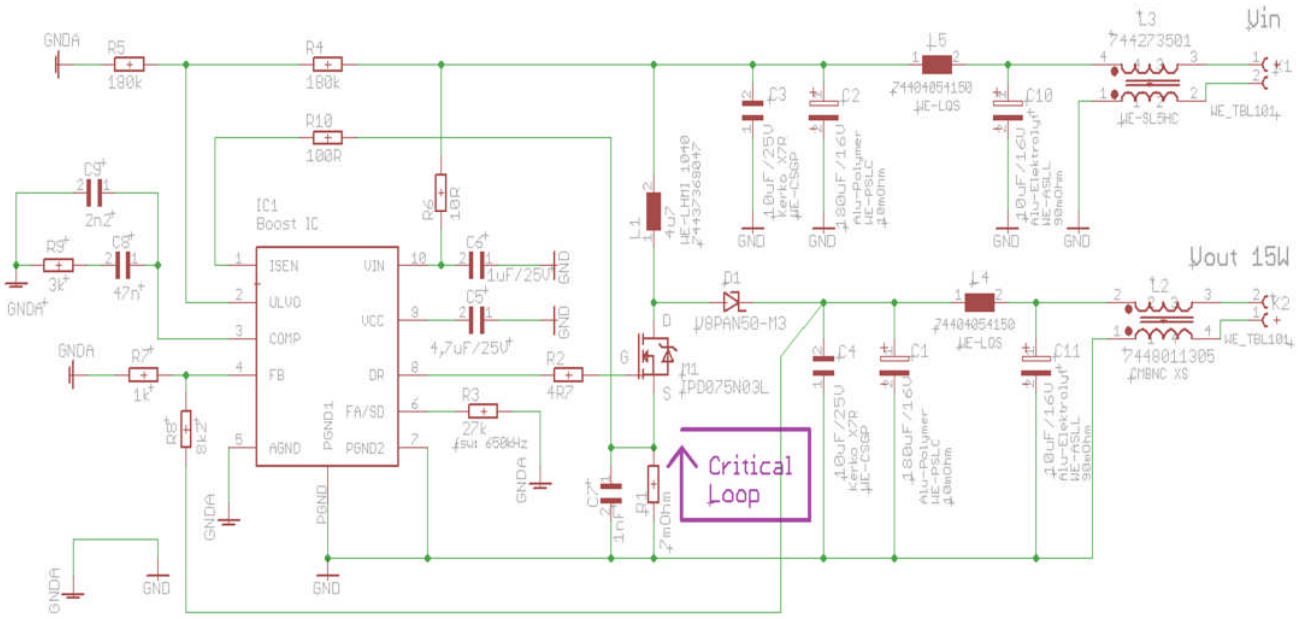


Fig. 15: Circuit diagram of a good design (Design 2) with Uin = 9 V, Uout = 12 V, Iout = 1.25 A, fsw = 650 kHz

Initial analysis of the circuit diagram for Design (2):

- Input and output capacitors are a combination of low-ESR MLCC (WCAP-CSGP) and low-ESR polymer capacitors (WCAP-PSLC only 180 µF).
- LC filters (WE-LQS & WCAP-ASLL) at the input and output of the boost converter.
- Series gate resistor at the external MOSFET.
- Shielded power choke WE-LHMI of the latest generation.
- Separation between AGND and PGND already apparent in the circuit diagram

Since this is an open design without shielding, current-compensated chokes (WE-CMBNC and WE-SL5HC) were also designed in, since common-mode interferences that decouple via stray capacitance. The selection criteria here are the maximum ampacity and a common-mode impedance that can set in from the switching frequency over as broad a bandwidth as possible.

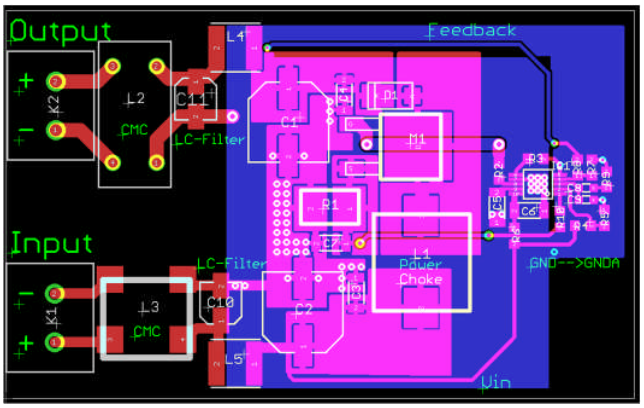


Fig. 16: Circuit-board layout of the good design (Design 2)

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Initial analysis of the circuit-board layout of Design (2):

- The PGND PTOs of the input and output capacitors, IC, and shunt R1 are located close to each other and already have a low-inductance connection at the TOP level via a copper surface (the critical loop is thus reduced to a minimum).
- The C5 and C6 blocking capacitors are positioned close to the IC and connected to the GND by an extremely low-inductance connection.
- All power connections are routed with connector tracks (or surfaces) that are as short and as broad as possible.
- Connection (at $C_{OUT} = C_2+C_4$) and routing (better laid-out bottom surface) of the feedback connector track is optimized.
- AGND and PGND are spatially separated and connected at a potentially quieter position.
- In general many vias are included, especially regarding the PGND connections, since each additional via reduces the parasitic inductance of the vias.
- Input and output connections are routed only via the filter components (thus no galvanic coupling).

2.6. MEASUREMENT OF THE INTERFERENCE SPECTRUM: CRITICAL DESIGN (DESIGN 1)

Measurement of the interference voltage, critical design (Design 1), without filter

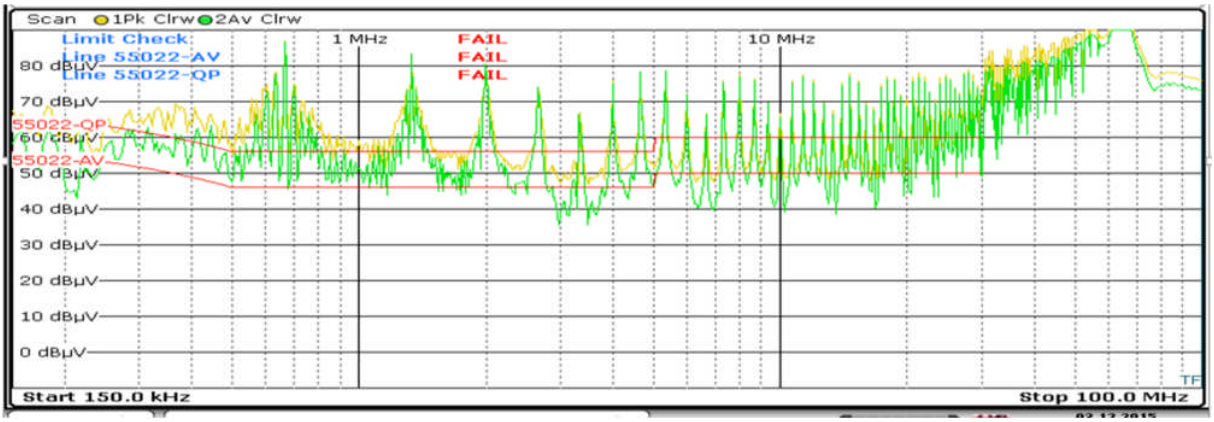


Figure 17: Measurement of the interference voltage of Design (1) at the output of the boost converter w/o filter

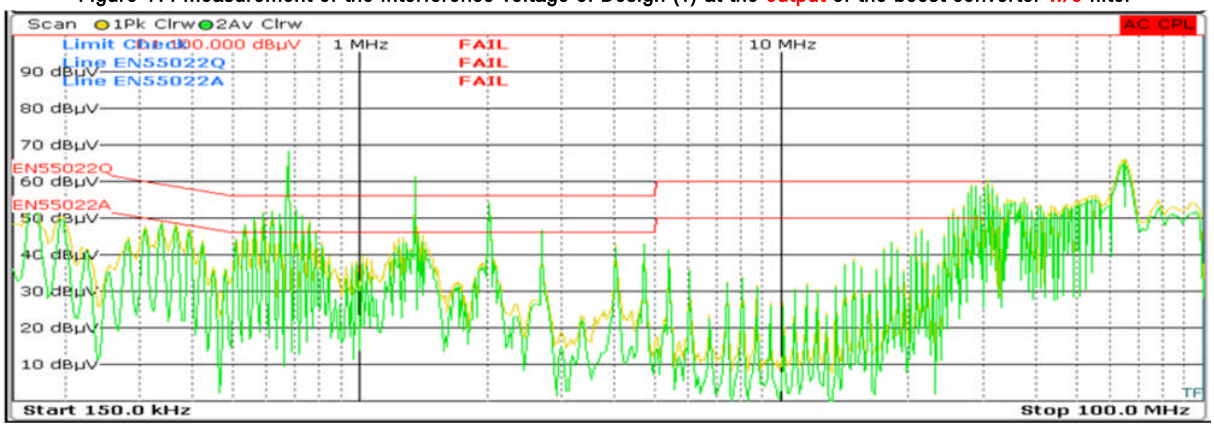
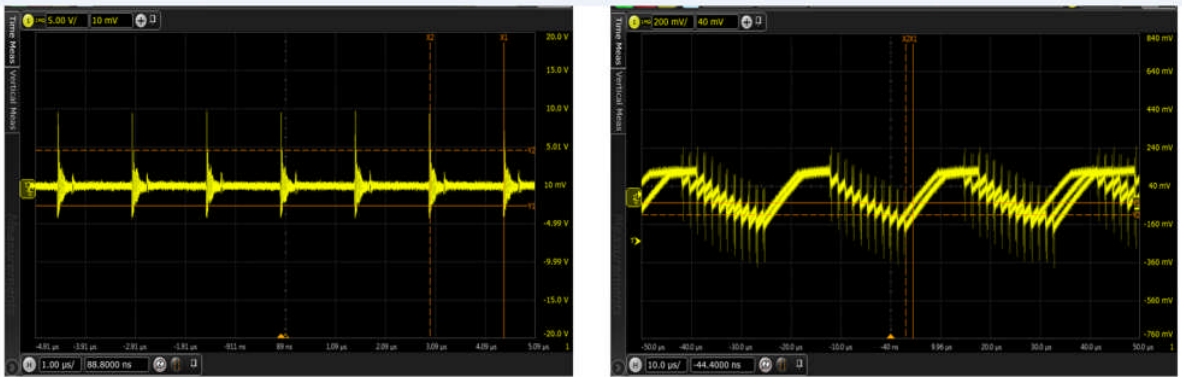


Figure 18: Measurement of the interference voltage of Design (1) at the input of the boost converter w/o filter

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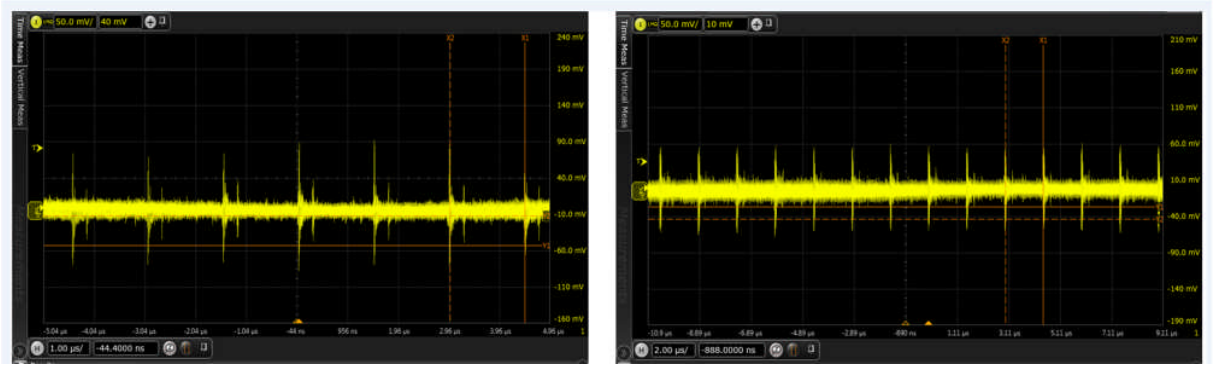
Output voltage (AC coupled) 5V/Div | Input voltage (AC coupled) 200mV/Div

Figure 19: Measurement of the interferences in the time domain of Design (1) at the input and output of the boost converter w/o filter

2.6.1. ANALYSIS (A) OF THE MEASUREMENTS OF THE CRITICAL DESIGN (DESIGN 1)

As assumed, the output of a boost switching controller is more critical regarding the expected level. Nevertheless, without further filtering the levels at the input are far too high. Measurements were made up to 100 MHz to obtain a trend for the levels in the measurement of the interference-field strengths (30 MHz to 400 MHz).

Measurement of the interference voltage, critical design (Design 1), with filter



Output voltage (AC coupled) 50mV/Div | Input voltage (AC coupled) 50mV/Div

Figure 20: Measurement of the interferences in the time domain of Design (1) at the input and output of the boost converter with LC filter (15 µH / 10 µF)

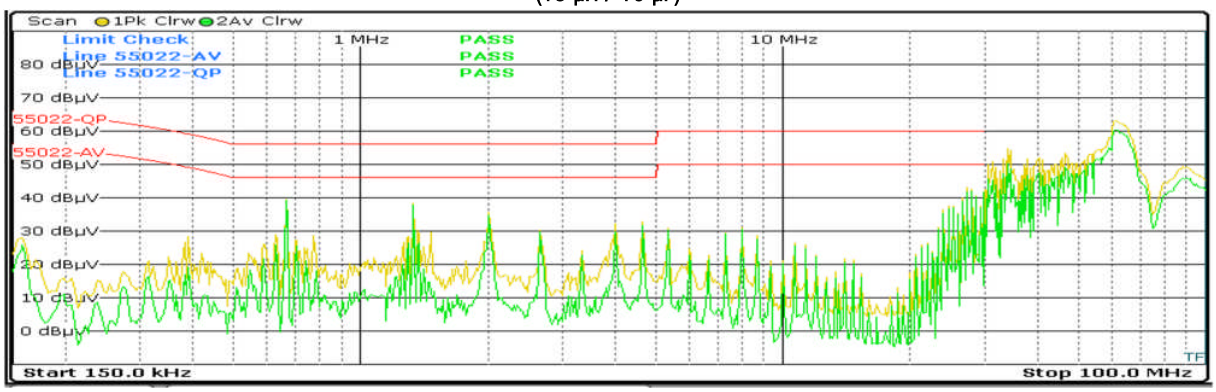


Figure 21: Measurement of the interference voltage of Design (1) at the output of the boost converter with LC filter (15 µH / 10 µF)

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

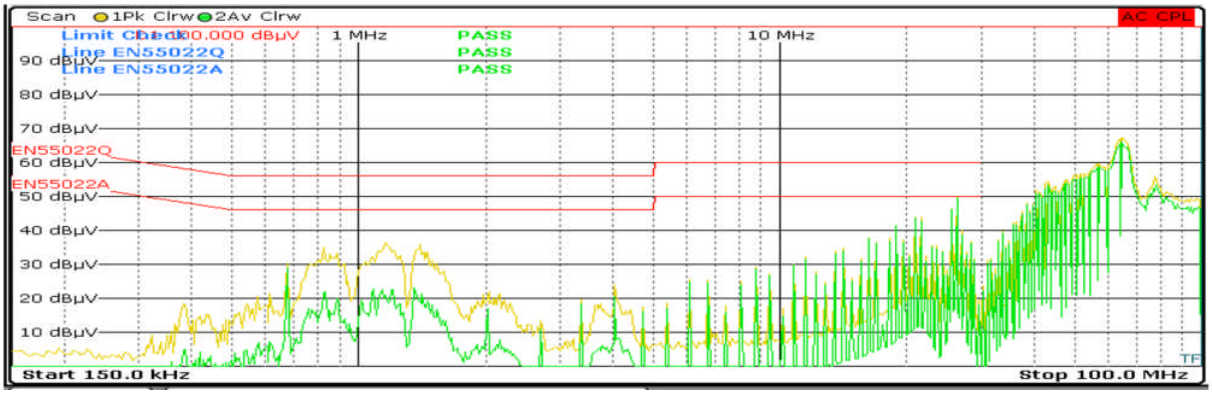


Figure 22: Measurement of the interference voltage of Design (1) at the input of the boost converter with LC filter (15 µH / 10 µF)

2.6.2. ANALYSIS (B) OF THE MEASUREMENTS OF THE CRITICAL DESIGN (DESIGN 1)

When a correspondingly large-dimensioned LC filter is used at the input and output of the boost converter, the level can be maintained up to 30 MHz and the interference-voltage measurement would be passed. The trend beyond 30 MHz, however, shows that problems must be reckoned with regarding the interference-field strength!

Measurement of the interference-field strength, critical design (Design 1)

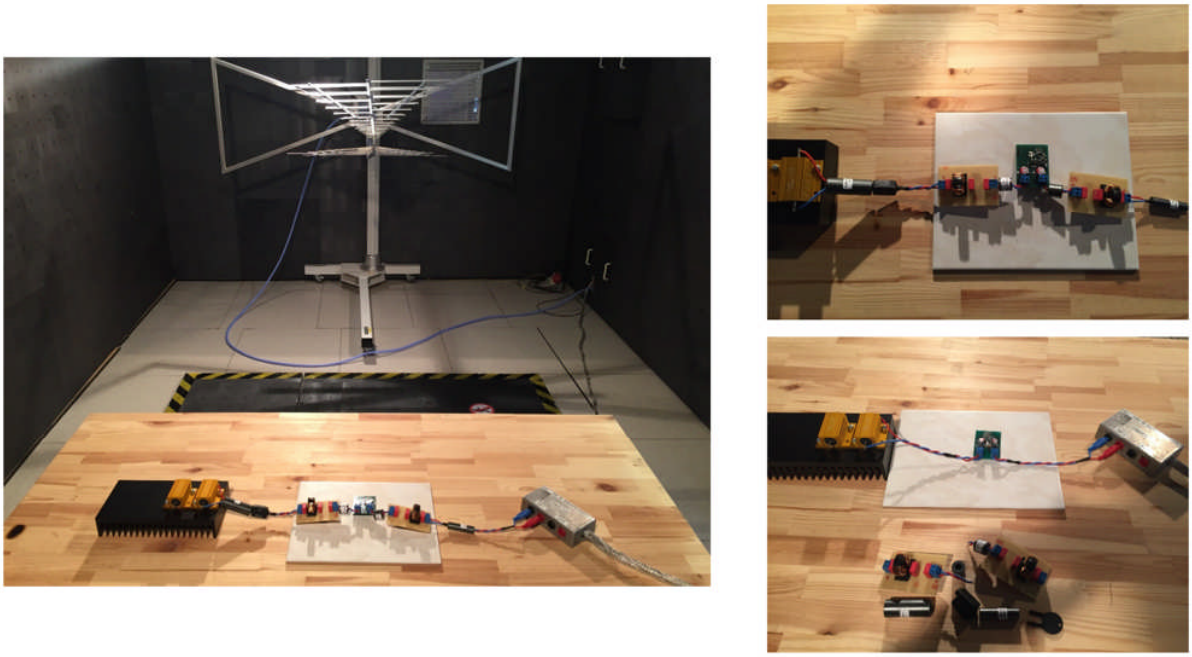


Fig. 23: Set-up for the measurement of the interference-field strength with and without external filters. The external filters should decouple the 20cm cable to ensure that only the emission of the circuit-board layout is measured

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

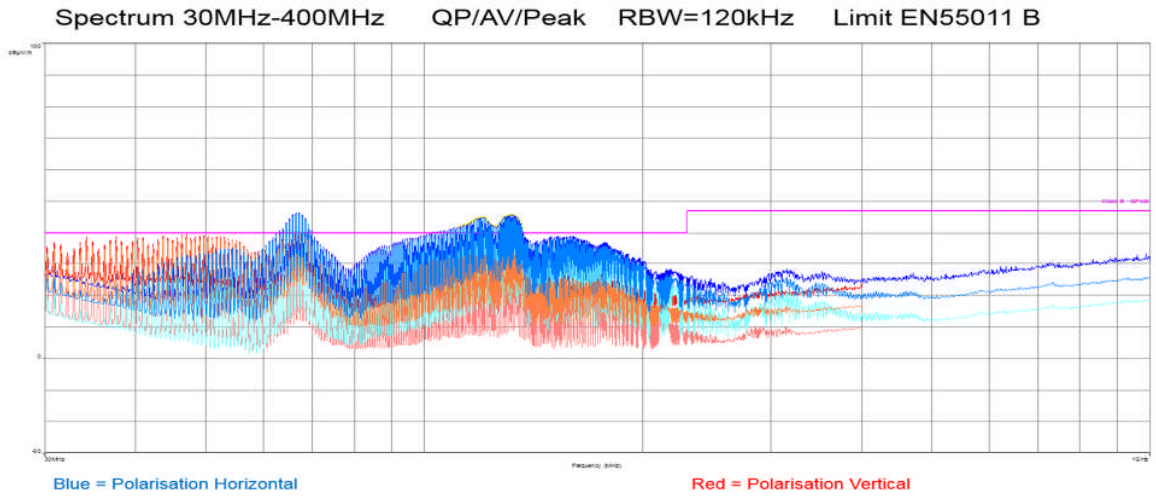


Fig. 24: Measurement of Design (1) with decoupling filters

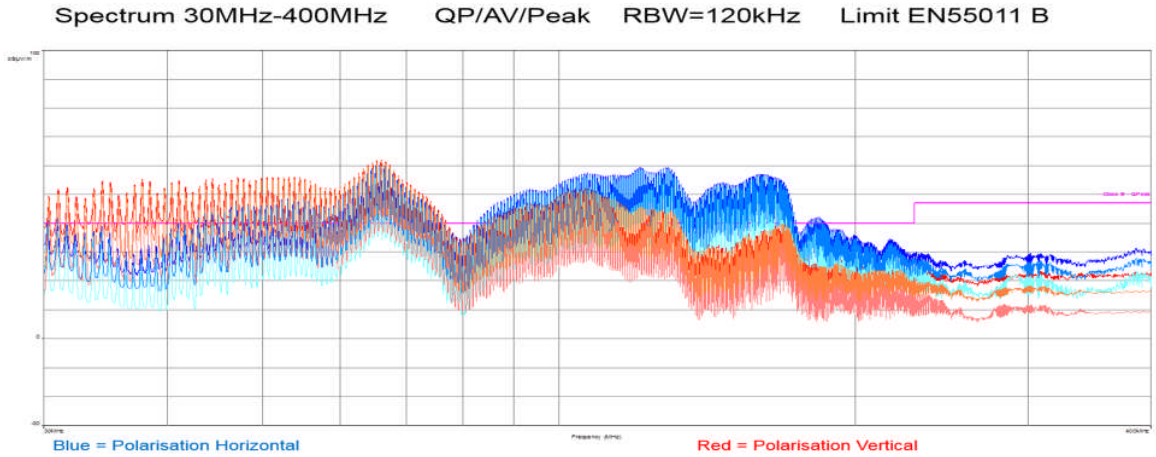


Fig. 25: Measurement of Design (1) w/o decoupling filters

2.6.3. ANALYSIS (C) OF THE MEASUREMENTS OF THE CRITCAL DESIGN (DESIGN 1)

As already assumed in the measurement of the interference voltage, the levels specified in EN 55011 Class B are exceeded. When a few more centimeters of cable are involved, the levels rise over a very broad bandwidth over 10…15 dBµV/m. This clearly illustrates the negative impact of the critical layout with the large critical current loops and with excessive parasitical inductance.

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

2.7. MEASUREMENT OF THE INTERFERENCE SPECTRUM: GOOD DESIGN (2)

Measurement of the interference voltage, good design (Design 2), without filter

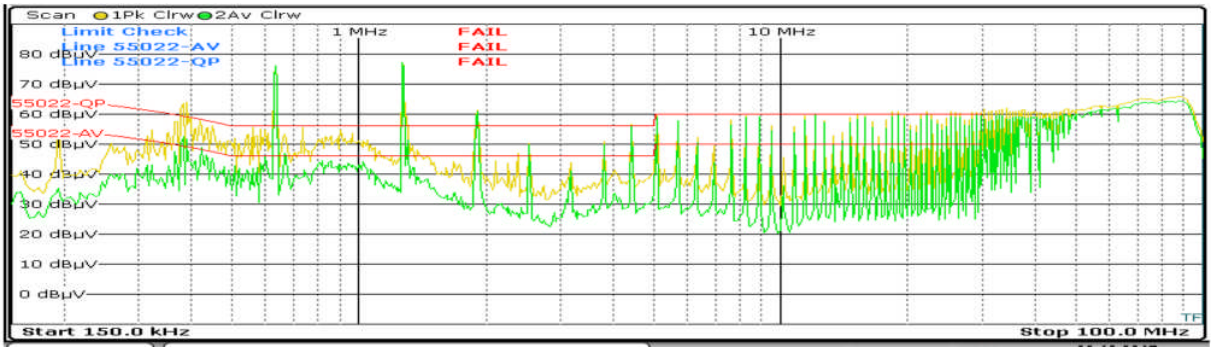


Figure 26: Measurement of the interference voltage of Design (2) at the output of the boost converter w/o filter

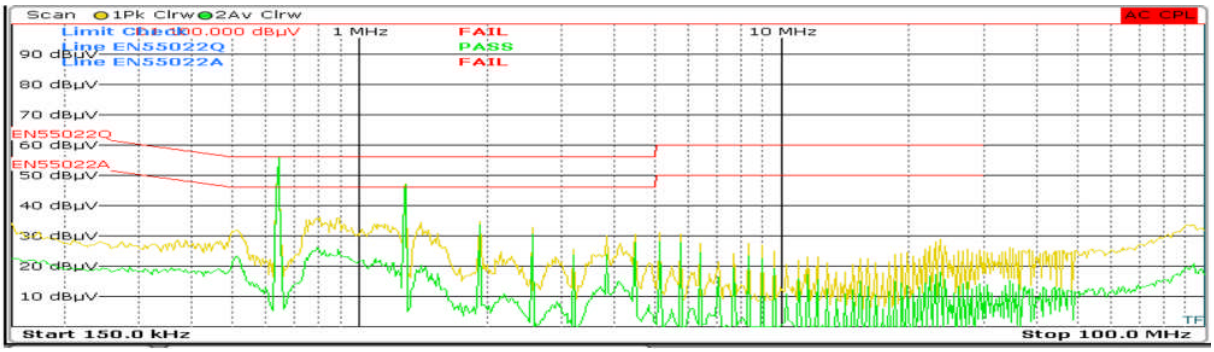
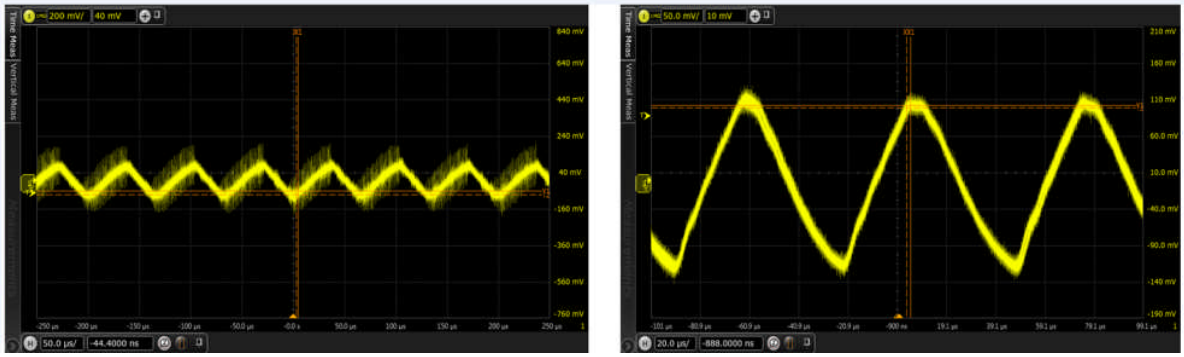


Figure 27: Measurement of the interference voltage of Design (2) at the input of the boost converter w/o filter



Output voltage (AC coupled) 200mV/Div

Input voltage (AC coupled) 50mV/Div

Fig. 28: Measurement of the interferences in the time domain of Design (2) at the input and output of the boost converter w/o filter

2.7.1. ANALYSIS (A) OF THE MEASUREMENTS OF THE GOOD DESIGN (DESIGN 2)

Measurement of the interference voltage, good design (Design 2), without filter

For the first measurements, the filters were temporarily removed from the good design so that only the input and output capacitors were still in place. The levels and the background noise in the measurement of the interference voltage are considerably better than those measured for the critical design (1). The voltage levels are also far lower in the time domain. Nevertheless, without filters even the good design does not succeed in fulfilling the class B limit specifications.

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Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

Measurement of the interference voltage, good design (Design 2), with filter

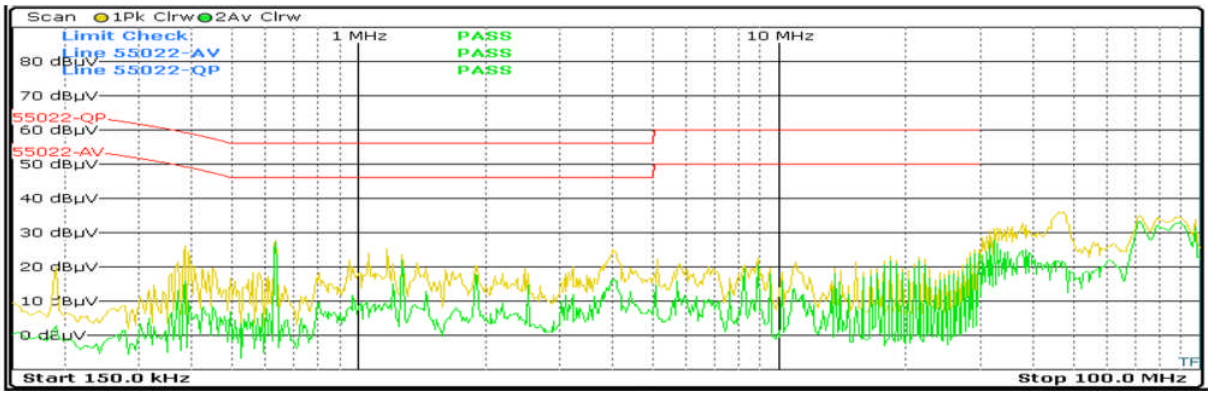


Figure 29: Measurement of the interference voltage of Design (2) at the output of the boost converter with filter (15 µH / 10µF / Stroko 5 mH)

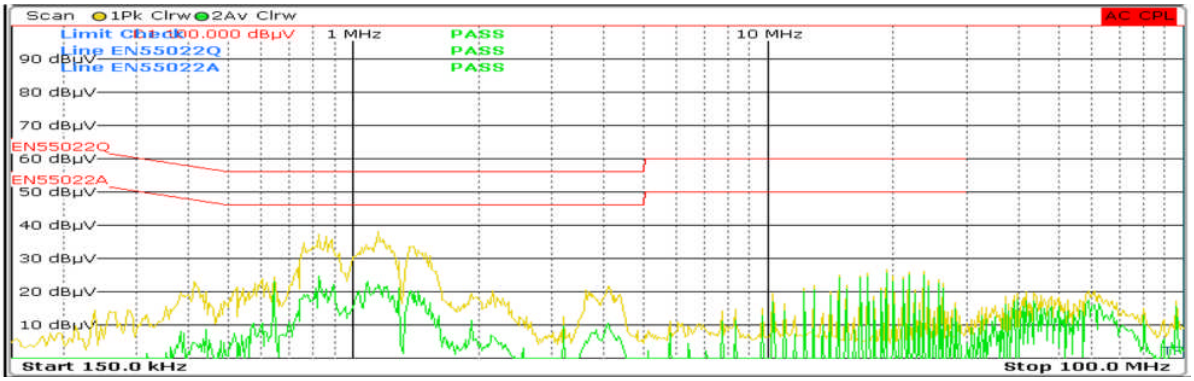
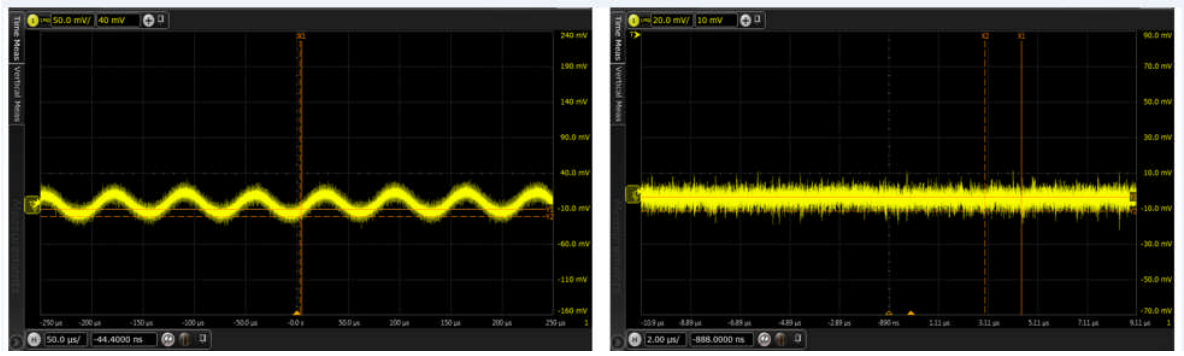


Figure 30: Measurement of the interference voltage of Design (2) at the input of the boost converter with filter (15 µH / 10 µF / Stroko 5 µH)



Output voltage (AC coupled) 50mV/Div

Input voltage (AC coupled) 20mV/Div

Fig. 31: Measurement of the interferences in the time domain of Design (2) at the input and output of the boost converter with filter

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

2.7.2. ANALYSIS (B) OF THE MEASUREMENTS OF THE GOOD DESIGN (DESIGN 2)

Equipped with the appropriate input and output filters, the good design (Design 2) is easily capable of fulfilling the class B limit specifications in the interference-voltage measurements. Due to the good layout, no major challenges are to be reckoned with above 30 MHz in the interference-field strength. The time domain too shows that the combination of the good layout and the right components results in a substantially less critical design.

Measurement of the interference-field strength, good design (Design 2)

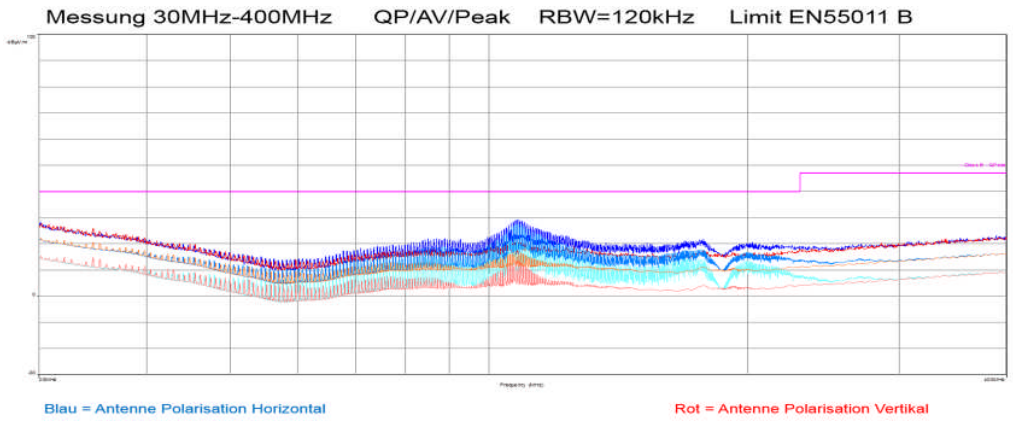


Figure 32: Measurement of design (2) with decoupling filters

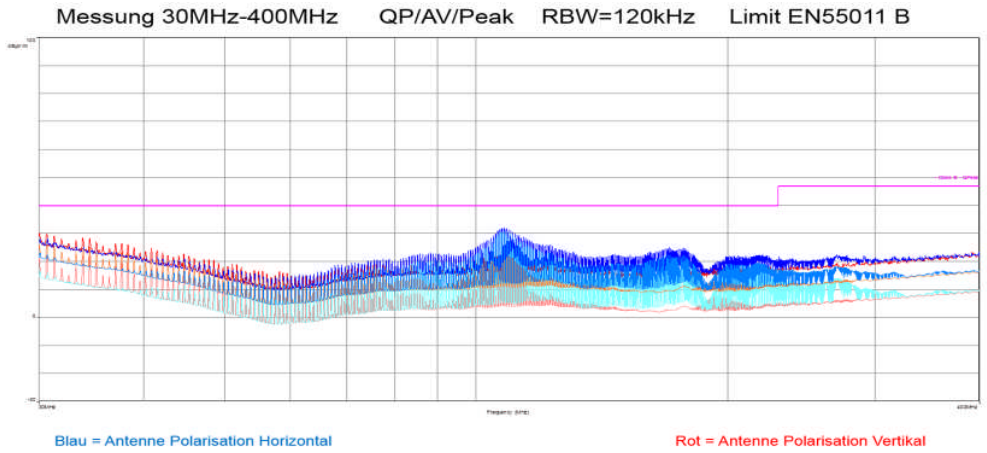


Figure 33: Measurement of design (2) w/o decoupling filters

2.7.3. ANALYSIS (C) OF THE MEASUREMENTS OF THE GOOD DESIGN (DESIGN 2)

As was already assumed in the measurement of the interference voltage, the limits specified in EN 55011 class B are fulfilled. Even when the approx. 20 cm length of cable is included, thanks to the better layout and the selected components the good design is capable of fulfilling the specifications.

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Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

2.8. MEASUREMENTS IN THE TIME DOMAIN ON THE CIRCUIT BOARDS



Figure 34: Measurement of the gate-source voltage at the MOSFET

High-frequency oscillations can be seen in the critical design, the result of an LC circuit formed by the gate capacitor in combination with the inductance of the thin and long connector track. What's more, the series gate resistor in the good design helps to brake the steep edge to a certain degree when the device is switched on.



Figure 35: Measurement of the drain-source voltage at the MOSFET

The critical design exhibits high-frequency oscillations when the device is switched on or off. These are due to an LC circuit formed by the drain-source capacitor (C_{DS}) in combination with the inductance of the thin connector tracks.

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

critical design approx. $40V_{pp}$

Good design approx. $19V_{pp}$



Figure 36: Measurement of the voltage over the Schottky diode

The reverse-recovery capacitance of the diode also causes very large high-frequency oscillations, which under certain circumstances may lead to the destruction of the diode or other components as a result of the high amplitude.

critical design approx. $2.2V_{pp}$

Good design approx. $90mV_{pp}$



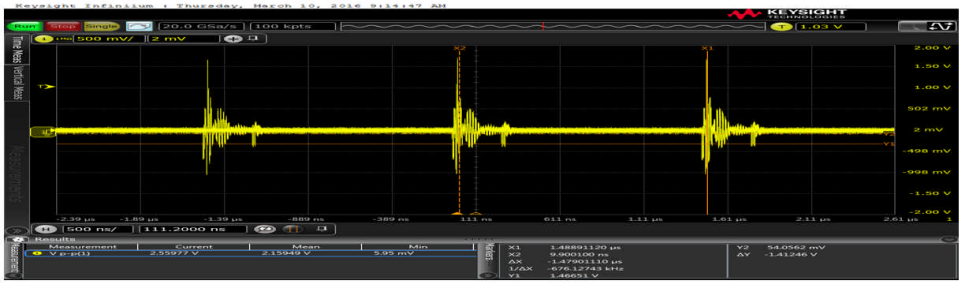
Figure 37: Measurement of the voltage at pin 10 (V_{IN}) of the boost IC

The fact that the blocking capacitor in the critical design is located approx. 3 mm away from pin 10 and connected only by a thin connector track means that the boost IC cannot draw the necessary current swiftly enough. The inductance of the thin connector track acts as a current brake, resulting in a high-frequency voltage with a large amplitude at this site (cf. Figs. 9 and 10).

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

critical design approx. $2.5V_{pp}$



Good design approx. $140mV_{pp}$

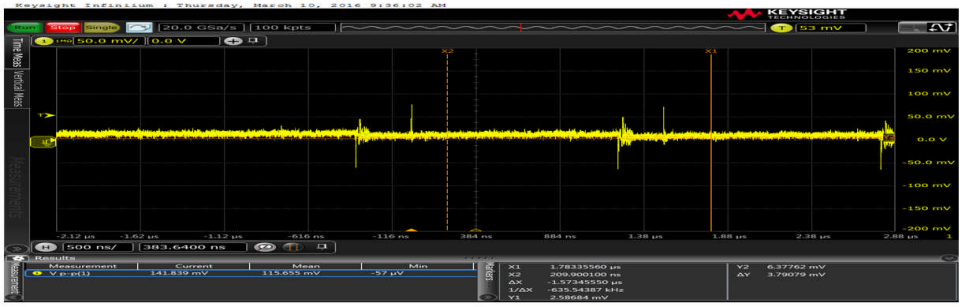


Figure 38: Measurement of the voltage at pin 9 (V_{CC}) of the boost IC

3. SUMMARY

The results of the measurements in the time domain and also in the frequency spectrum clearly show the impact made on the designs by the selection of the correct components, their position, small critical current loops, and a low track inductance layout. It is also evident that a very critical layout fails to fulfil the specifications for interference-field strength even when many filters are used. In such a case, the only way out is to completely shield the component, including the filtering of the leads.

For those who have only limited experience in the area of discrete switching controllers, and also for those who are not prepared to make the necessary investment of time and effort into dealing with the matter, a highly integrated power module (WE Magic³ Power Module) represents an interesting alternative. Only a few design steps and a short time investment are necessary to achieve a swift result – one that is also less critical in terms of EMC – when the specifications of the data sheet are observed.

4. PART LIST OF THE FILTER COMPONENTS FOR DESIGN (2)

Index	Beschreibung	Bauform	Wert	Artikelnummer
L4/L5	WE-LQS	5 x 5 x 4mm³	15µH, 2A	744 040 541 50
L2	WE-CMBNC	XS	5mH, 1,3A	744 801 130 5
C12	WCAP-CSGP	1206	10µF, 25V, X7R	885 012 208 069
C1/C2	WCAP-PSLC	8mm x 11,7mm	180µF, 16V, 105°C, 2000h	875 075 355 001
L3	WE-SL5HC	9,5 x 8,3 x 5,3mm³	5µH, 5A	744 273 501
C10	WCAP-ASLL	4mm x 5,5mm	10µF, 16V, 105°C, 2000h	865 060 340 001

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

5. ANNEX

5.1. REFERENCES

Related links for further details: Negative input resistance

(1) ANP008: Negative input resistance of switching regulators
www.we-online.com/anp008

(2) Input filter interaction
http://www.smpstech.com/filter00.htm

(3) SNVA489C: Input Filter Design for Switching Power Supplies
http://www.ti.com.cn/cn/lit/an/snva489c/snva489c.pdf

(4)Trilogy of Magnetics
http://www.we-online.de/web/de/electronic_components/produkte_pb/fachbuecher/fachbuecher.php

(5) RHPZ analysis
http://www.ti.com/lit/an/slva274a/slva274a.pdf

Application Note

Impact of the layout, components, and filters on the EMC of modern DC/DC switching controllers

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USEFUL LINKS

Application Notes:
http://www.we-online.com/app-notes

REDEXPERT Design Tool:
http://www.we-online.com/redexpert

Toolbox:
http://www.we-online.com/toolbox

Product Katalogue:
http://katalog.we-online.com

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