Agenda

- Background
- Design overview
- Vendor deployment
- Current status
- Next steps
Hierarchical PM topology

- CPUs, integrated devices, power domains, micro controllers, firmware etc
CPU subsystem
CPU cluster idle

PROBLEM:

- CPUIdle manages CPUs well, but does not scale for multi-cluster SMP systems and heterogeneous systems like big.LITTLE.

SOLUTION:

- For devices in general: Idle management via runtime PM + generic PM domain (aka genpd) - a proven method!
- For a modern SoC with hierarchical PM topology, let’s use/extend runtime PM and genpd to cope with CPUs.
- An important side-effect, a unified solution for idle management across all kind of devices.
CPU cluster idle - problem

- CPUs
- Cluster
- Coherency
- CPU Idle
- Platform hacks
CPU cluster idle - solution
CPU PM domain

- PSCI_FEATURES read from firmware.
- Deployment needs PSCI OSI mode!
- Using PSCI composite state-ID.
- CPU PM domains topology soaked in via DT.
- CPU PM domain governor to select idle state.

No vendor specific code needed for ARM64, only the description in DT!
Current status

- Define DT bindings for domain idle states (merged).
- Parse domain idle states for DT in genpd (merged).
- IRQ-safe domain support for genpd (merged, review).
- Runtime PM deployment for CPUIdle (review).
- CPU PM domains (review).
- Implementation for ARM64 using PSCI 1.0 (review).
- DT for ARM64 Dragonboard 410C (review).
- DT for MediaTek EVB Boards (to be posted).
Next steps

- Deploy CPU PM domain approach for an ARM32 SoC.
- Use IRQ based next event prediction in the CPU PM domain governor.
- Optimize runtime PM path when used for CPUs.
- Replace CPU PM notifications with runtime PM callbacks.
Thank You

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